Electronic Version
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Description

Self-Biasing Differential Buffer with Transmission-Gate Bias Generator

BACKGROUND OF INVENTION

[0001] This invention relates to differential buffers, and more particularly to self-biasing of differential buffers.

[0002] Differential buffers are a widely used building block in electronic systems. Input signals can be fully differential, with a true and a second, complement line that are driven to opposite states. Many kinds of low-voltage differential signaling (LVDS) have been developed and are available.

[0003] Differential buffers can also be used with single-ended input signals. The single input signal is compared to a reference voltage by the differential buffer. The reference voltage can be applied to the inverting (negative) input of the differential buffer while the input signal is applied to the non-inverting (positive) input.

[0004] Figure 1 shows a differential buffer comparing an input signal to a reference voltage. Differential buffer 10 re-

ceives an input signal DIN on the non-inverting (+) input, and a reference voltage VREF on its inverting (-) input. Output Q is driven high when the input voltage of DIN is above VREF; otherwise output Q is driven low by differential buffer 10.

[0005] The reference voltage VREF can be set to the logic threshold level of input signal DIN. This switching threshold is often set to be half of the power-supply voltage, or VDD/2. Reset signal RST can be activated to reset the output.

[0006] Internal bias voltages are often used in complementary metal-oxide-semiconductor (CMOS) amplifiers and buffers. A voltage divider between power and ground can generate one or more bias voltages that are applied to gates of current source transistors in the differential amplifier. The voltage divider often is a series connection of transistors, and may include one or more resistors in series with the transistors.

[0007] The voltage divider generating the bias voltages has the disadvantage of no feedback to compensate for temperature, power-supply, and process variations.

[0008] What is differential buffer that generates its own bias voltages without an input from a voltage divider between power and ground. A self-biased differential buffer is de-

sirable.

Brief Description of Drawings

[0009] Figure 1 shows a differential buffer comparing an input signal to a reference voltage.

[0010] Figure 2 is a schematic of a simplified self-biased differential buffer with a single output.

[0011] Figure 3 is a schematic of a balanced differential buffer core with transmission gates that generate a self-bias voltage.

[0012] Figure 4 shows output buffering around the buffer core.

Detailed Description

[0013] The present invention relates to an improvement in self-biasing differential buffers. The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent

with the principles and novel features herein disclosed.

[0014] The inventor has realized that bias voltages can be generated from the differential inputs rather than from a separate voltage divider between power and ground. A common-mode voltage is generated between the two differential inputs. The differential inputs are buffered and applied to transmission gates. A node between two transmission gates is used as the self-generated bias voltage.

[0015] Figure 2 is a schematic of a simplified self-biased differential buffer with a single output. This simplified embodiment does not use transmission gates or differential outputs.

[0016] Reference voltage VREF is compared to the DIN signal input voltage by the buffer. Reference voltage VREF is applied to the gates of p-channel reference transistor 32 and n-channel reference transistor 34. The drains of reference transistors 32, 34 are tied together and generate the self-bias voltage VB. Self-bias voltage VB is fed back to the gates of p-channel current-source transistor 30 and n-channel current-sink transistor 44.

[0017] Reset transistor 42 is an n-channel transistor receiving reset signal RSTB at its gate, and cuts off current flow in the differential buffer when reset is active and RSTB is low.

Reset transistor 42 conducts between the sources of transistors 34, 38 and n-channel current-sink transistor 44 to ground.

[0018] The data input signal DIN is applied to the gates of p-channel input transistor 36 and n-channel input transistor 38. The drains of input transistors 36, 38 drive an input of NAND gate 40, which drives output Q. The other input of NAND gate 40 is the active-low reset signal RSTB. When reset is active, NAND gate 40 drives Q high, blocking the data.

[0019] Current from p-channel current-source transistor 30 divides into two branches. One branch through reference transistors 32, 34 sets the self-reference voltage VB, while the other current branch through input transistors 36, 38 drives the output. The two branch currents are combined at the drain of reset transistor 42 and the current sunk is set by n-channel current-sink transistor 44, since VB is usually less than RSTB, which is usually at VDD.

[0020] When DIN is higher than VREF, n-channel input transistor 38 tends to conduct more current than n-channel reference transistor 34. Also, p-channel input transistor 36 tends to conduct less than p-channel reference transistor 32, for equal-sized transistors. This causes the input to

NAND gate 40 to fall, driving Q high.

[0021] Self-bias voltage VB also rises somewhat. The rising VB increases current sunk in n-channel current-sink transistor 44 but decreases the current sourced by p-channel current-source transistor 30. This helps to lower VB, compensating for the rise in VB due to DIN rising above VREF. Thus the self-bias voltage is self-compensating.

[0022] When DIN is lower than VREF, n-channel input transistor 38 tends to conduct less current than n-channel reference transistor 34. Also, p-channel input transistor 36 tends to conduct more current than p-channel reference transistor 32, for equal-sized transistors. This causes the input to NAND gate 40 to rise, driving Q low.

[0023] Self-bias voltage VB also falls somewhat. The falling VB decreases current sunk in n-channel current-sink transistor 44 but increases the current sourced by p-channel current-source transistor 30. This helps to raise VB, compensating for the fall in VB due to DIN falling below above VREF. The self-bias voltage is again self-compensating.

[0024] The self-compensation of self-bias voltage VB is due to a feedback mechanism. Since VB tends to remain constant, the propagation delay through the differential buffer remains relatively constant, despite shifts in input voltage

DIN. Having a relatively constant propagation delay is useful in some applications, since it reduces variation in output timing.

[0025] The amplification or gain from VREF to Q is much smaller than the gain from input DIN to Q, since the drains of DIN input transistors 36, 38 drive NAND gate 40 to the output, while reference transistors 32, 34, which receive input VREF, are not directly connected to NAND gate 40. A large voltage change in VREF produces a very small change in Q, since any changes in VREF have to couple through p-channel current-source transistor 30 or n-channel current-sink transistor 44.

[0026] The energy of input VREF is mostly used to generate the self-bias referenced voltage VB, with little of the input energy going to output Q. In contrast, most of the energy from input DIN is used to generate the Q output.

[0027] While the differential buffer of Fig. 2 is useful when one input is a reference voltage that does not carry a varying small signal, the differential buffer is not useful when both inputs carry varying input signals, such as for a full differential signal. The self-bias voltage is more sensitive to the reference voltage VREF than to the DIN input voltage. A more balanced self-biasing differential buffer is

desirable.

[0028] Figure 3 is a schematic of a balanced differential buffer core with transmission gates that generate a self-bias voltage. Buffer core 70 has two input amplifiers. One input amplifier received data input DIN, while the other receives the reference voltage VREF. The two input amplifiers are coupled together by transmission gates to generate the self-bias voltage VB.

[0029] Each input amplifier has two current branches. One branch carries a higher current and drives output buffers, while the other branch carries a smaller current, and drives the transmission gate to generate the self-bias voltage. Thus most of the amplifier's energy is directed to generating the output, with a small amount of the energy for generating the self-bias voltage. For example, 10% of the energy may go toward self-bias generation, with 90% of the energy going toward output generation.

[0030] The DIN input amplifier has p-channel reference transistor 46 receiving self-bias voltage VB at its gate, to source a current through p-channel reset transistor 48 to the upper branching node. N-channel current-sink transistor 66 also receives self-bias voltage VB at its gate, and sinks a current from the lower branching node through n-channel

reset transistor 64.

[0031] One current branch between the upper and lower branching nodes passes through p-channel drive transistor 50 and n-channel drive transistor 52, which both receive input DIN at their gates. The drains of drive transistors 50, 52 drive the QBOUT output. Most of the current from p-channel reference transistor 46 passes through this branch.

[0032] A second current branch between the upper and lower branching nodes passes through p-channel bias-generating transistor 54 and n-channel bias-generating transistor 56, which both receive input DIN at their gates. The drains of bias-generating transistors 54, 56 drive a transmission gate of p-channel transistor 62 and n-channel transistor 60. The other side of this transmission gate is the self-bias voltage VB. Thus this second current branch is used to generate the self-bias voltage. A smaller current passes through bias-generating transistors 54, 56 than through drive transistors 50, 52, since transistors 50, 52 can have a larger size (W/L) than transistors 54, 56. For example, transistors 50, 52 can have ten times the width of transistors 54, 56. Thus little energy is used for generating the self-bias voltage VB.

[0033] The VREF input amplifier has p-channel reference transistor 146 receiving self-bias voltage VB at its gate. Reference transistor 146 sources a current through p-channel reset transistor 148 to the upper branching node. N-channel current-sink transistor 166 also receives self-bias voltage VB at its gate, and sinks a current from the lower branching node through n-channel reset transistor 164.

[0034] One current branch between the upper and lower branching nodes passes through p-channel drive transistor 150 and n-channel drive transistor 152, which both receive input VREF at their gates. The drains of drive transistors 150, 152 drive the QOUT output. Most of the current from p-channel reference transistor 146 passes through this branch.

[0035] A second current branch between this amplifier's upper and lower branching nodes passes through p-channel bias-generating transistor 154 and n-channel bias-generating transistor 156, which both receive input VREF at their gates. The drains of bias-generating transistors 154, 156 drive a transmission gate of p-channel transistor 162 and n-channel transistor 160. The other side of this transmission gate is the self-bias voltage VB. Thus this second current branch is used to generate the self-

bias voltage. A smaller current passes through bias-generating transistors 154, 156 than through drive transistors 150, 152, since transistors 150, 152 can have a larger size (W/L) than transistors 154, 156.

[0036] The differential buffer is symmetric. Inputs DIN and VREF can be interchanged. Rather than have a fixed reference voltage, a time-varying differential signal can be applied to the VREF input as well as the DIN input. The energy directed toward the bias generation is roughly the same for both inputs, since the circuit is balanced.

[0037] The circuit can be powered down by activating reset. Inverter 58 generates active-high RST from an active-low input RSTB. When RSTB is low (active), n-channel reset transistors 64, 164 turn off, and n-channel transmission gate transistors 60, 160 also turn off, allowing VB to float. During reset, RST is high, and p-channel reset transistors 48, 148 and p-channel transmission gate transistors 62, 162 all turn off. Current flow from power through transistors 62, 162, 80, 90 (Fig. 4) is halted during reset by these transistors turning off. When reset is inactive, these transistors are turned on.

[0038] Figure 4 shows output buffering around the buffer core. Buffer core 70, shown in Fig. 3, generates differential out-

puts QOUT, QBOUT. QOUT is pulled low by n-channel reset transistor 90 when reset signal RST is high. QBOUT is pulled high by p-channel reset transistor 80 when reset signal RSTB is low.

[0039] When reset is off, QOUT is inverted by first inverting transistors 82, 86. The drains of first inverting transistors 82, 86 are applied to the gates of second inverting transistors 84, 88, which drive output Q from their drains.

[0040] QBOUT is inverted by first inverting transistors 74, 78 when reset is off. The drains of first inverting transistors 74, 78 are applied to the gates of second inverting transistors 72, 76, which drive output QB from their drains.

[0041] For a power-supply voltage of 1.8 volts, the input signal can vary from 0.675v to 1.125v with minimal change in output delay. Other voltages and common-mode ranges are possible.

[0042] ALTERNATE EMBODIMENTS

[0043] Several other embodiments are contemplated by the inventors. For example, different transistors sizes and shapes could be used, and in differing ratios. The differential buffer could receive a clock signal, or a data or control signal as the data input DIN. Additional components such as capacitors and resistors could be added, and ac-

tive buffers and inverters could be added. The differential outputs or inputs could be swapped, buffered, or inverted. Various transistor sizes could be used, and transistors could be ratioed in size to ratio currents. A full differential signal D+, D-, rather than DIN and VREF could be input to the balanced self-biasing differential buffer. Thus VREF could be replaced by DIN- in Figs. 3, 4.

[0044] When there is no requirement for a power-down mode, several transistors can be deleted. Without a power-saving or rest mode, transistors 60, 62, 160, 162, 48, 148, 64, 164 may be deleted.

[0045] Any advantages and benefits described may not apply to all embodiments of the invention. When the word "means" is recited in a claim element, Applicant intends for the claim element to fall under 35 USC Sect. 112, paragraph 6. Often a label of one or more words precedes the word "means". The word or words preceding the word "means" is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means-plus-function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw

have different structures, they are equivalent structures since they both perform the function of fastening. Claims that do not use the word "means" are not intended to fall under 35 USC Sect. 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0046] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.